REMARKS

This paper is responsive to the Office Action dated April 23, 2007. Claims 5-7, 12, 13 and 17-19 are currently pending in the subject application. Claims 5-7, 12, 13 and 17-19 have been amended. Support for all amended claims can be found in the specification, and no new matter has been added by these amendments. Reconsideration of the claims in view of the amendments and the following remarks is respectfully requested.

Examiner Interview

Applicants gratefully acknowledge the telephone conference between the Examiner and Applicants' representative on August 30, 2007, during which certain differences between proposed claims and the cited references were discussed.

Claim Objections

The Office Action objected to claims 13, 17 and 19 due to informalities. Specifically, claims 13 and 19 were objected to because "the address" lacks antecedent basis. Furthermore, claim 17 was objected to because "the information processor" lacks antecedent basis. Applicants have amended the claims in accordance with the suggestion of the Examiner. Thus, the informalities have been corrected and the objection to the claims is overcome.

Claim Rejections Under 35 U.S.C. § 112

The Office Action rejected claims 5-7, 12, and 17-19 under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Specifically, several elements in the claims lack antecedent basis. Applicants have amended the claims in accordance with the suggestion of the Examiner. Accordingly, Applicants respectfully request withdrawal of the rejection of claims 5-7, 12, and 17-19 under 35 U.S.C. 112.

Claim Rejections Under 35 U.S.C. § 103

The Office Action rejected claims 5, 6, 12, 17 and 18 under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,724,501 issued to *Dewey* in view of U.S. Patent

Publication No. 2002/0107667 to *Mathiske*. The Office Action further rejected claims 5 and 17 under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent Publication No. 2002/107667 to *Ninomiya* in view of *Dewey* and *Mathiske*. The Office Action further rejected claims 7, 13 and 19 under 35 U.S.C. 103(a) as being unpatentable over *Dewey* and *Mathiske* in view of U.S. Patent No. 5,155,828 issued to *La Fetra*. Without conceding the merits of the rejection, Applicants respectfully submit that the amended claims overcome these rejections.

Claims 5-7, 12, 13 and 17-19 have been amended to include a feature of the invention described in the specification with reference to Figure 18. For example, claim 5, as amended, recites in part, "writing data in the first local cache memory and the second local cache memory which is not yet reflected to the global cache memory out to the global cache memory to reflect the data into the global cache memory; removing power from the first channel control unit and the second channel control unit after the data is reflected into the global cache memory; writing data in the global cache memory which is not yet reflected to the disk drive out to the disk drive to reflect the data into the disk drive; and removing power from the global cache memory, the disk control unit, and the disk drive after the data is reflected to the disk drive."

The amended claims are directed to a storage system which duplicates data on channel control units to secure a faster response to a host computer and data redundancy under normal conditions. The storage system maintains data consistency during a destage process when an emergency destaging process is required. Data integrity is also maintained using a global cache memory when a failure occurs in another global cache memory during the emergency destaging process.

In contrast, *Dewey* discloses a single dump link connecting memories on two units. (Column 12, lines 23-24). Data is replicated between controller units for fault tolerance. (Column 5, lines 18-33). *Dewey* does not teach decentralization of cache memories in case of a performance problem of global cache memories and a corresponding connecting means.

Mathiske teaches a thread local store buffer and a global store buffer. When the thread local store buffer overflows, the local store buffer is flushed to the global store buffer. (Paragraph [0036]). This is different than the invention recited in claim 5.

Ninomiya teaches cache memories arranged in a duplexed form. A common bus is provided between logical units and a memory divided into two channels. When one of the logical units becomes faulty, the other unit may be used to perform a degrade operation. Information indicative of the degraded operation status at the time of a failure is written in the shared memory. (Paragraph [0009]). *Ninomiya* does not disclose the implementation of cache memories on channel control units. Nor does *Ninomiya* teach controlling techniques of the cache memories.

La Fetra discloses a cache controlling method for use by a processor to control a cache memory. (Column 2, lines 11-36). This is different than a disk control apparatus for controlling a cache memory.

Neither *Dewey*, *Mathiske*, *Ninomiya*, *La Fetra* nor any of the other cited references, alone or in combination, teach or suggest all of the features recited in independent claim 5. Specifically, *Dewey*, *Mathiske*, *Ninomiya* and *La Fetra* do not teach or suggest "writing data in the first local cache memory and the second local cache memory which is not yet reflected to the global cache memory out to the global cache memory to reflect the data into the global cache memory; removing power from the first channel control unit and the second channel control unit after the data is reflected into the global cache memory; writing data in the global cache memory which is not yet reflected to the disk drive out to the disk drive to reflect the data into the disk drive; and removing power from the global cache memory, the disk control unit, and the disk drive after the data is reflected to the disk drive," as recited in claim 5. For at least this reason, claim 5 is allowable over the cited art.

Applicants have amended independent claims 6, 7, 12, 13 and 17-19 to recite features that are similar to the features recited in amended claim 5. As discussed above with reference to claim 5, the cited art does not teach or suggest these features. Thus, claims 6, 7, 12, 13 and 17-19 are also allowable over the cited art for at least the same reasons.

Accordingly, Applicants respectfully request withdrawal of the rejection of claims 5-7, 12, 13 and 17-19.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400.

Respectfully submitted,

8/30/07
Date

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